

# NCP5355

## 12 V Synchronous Buck Power MOSFET Driver

The NCP5355 is a dual MOSFET gate driver optimized to drive the gates of both high- and low-side Power MOSFETs in a Synchronous Buck converter. The NCP5355 is an excellent companion to multiphase controllers that do not have integrated gate drivers, such as ON Semiconductor's NCP5314 or NCP5316. This architecture provides the power supply designer greater flexibility by being able to locate the gate drivers close to the MOSFETs.

Driving MOSFETs with a 12 V source as opposed to a 5.0 V can significantly reduce conduction losses. Optimized internal, adaptive nonoverlap circuitry further reduces switching losses by preventing simultaneous conduction of both MOSFETs.

The floating top driver design can accommodate MOSFET drain voltages as high as 26 V. Both gate outputs can be driven low by applying a low logic level to the Enable (EN) pin. An Undervoltage Lockout function ensures that both driver outputs are low when the supply voltage is low, and a Thermal Shutdown function provides the IC with overtemperature protection.

The NCP5355 has the same pinout as the NCP5351 5.0 V Gate Driver.

### Features

- 8.0 V – 14 V Gate Drive Capability
- 2.0 A Peak Drive Current
- Rise and Fall Times < 15 ns Typical into 3300 pF
- Propagation Delay from Inputs to Outputs < 30 ns
- Adaptive Nonoverlap Time Optimized for Large Power MOSFETs
- Floating Top Driver Accommodates Applications Up to 26 V
- Undervoltage Lockout to Prevent Switching when the Input Voltage is Low
- Thermal Shutdown Protection Against Overtemperature
- TG to DRN Pulldown Resistor Prevents HV Supply-Induced Turn-On of Top MOSFET
- BG to PGND Pulldown Resistor Prevents Transient Turn On of Bottom MOSFET
- Internal Bootstrap Diode Reduces Parts Count and Total Solution Cost
- Pb-Free Package is Available



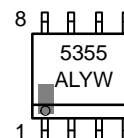
ON Semiconductor®

<http://onsemi.com>

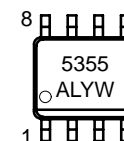
### MARKING DIAGRAMS



SOIC-8  
D SUFFIX  
CASE 751

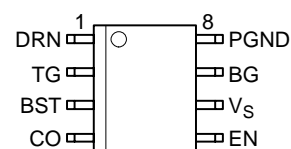


SOIC-8 EP  
D SUFFIX  
CASE 751AC



A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week

### PIN CONNECTIONS



### ORDERING INFORMATION

Device	Package	Shipping†
NCP5355D	SOIC-8	98 Units/Rail
NCP5355DR2	SOIC-8	2500 / Tape & Reel
NCP5355DR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel
NCP5355PDR2	SOIC-8 EP	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NCP5355

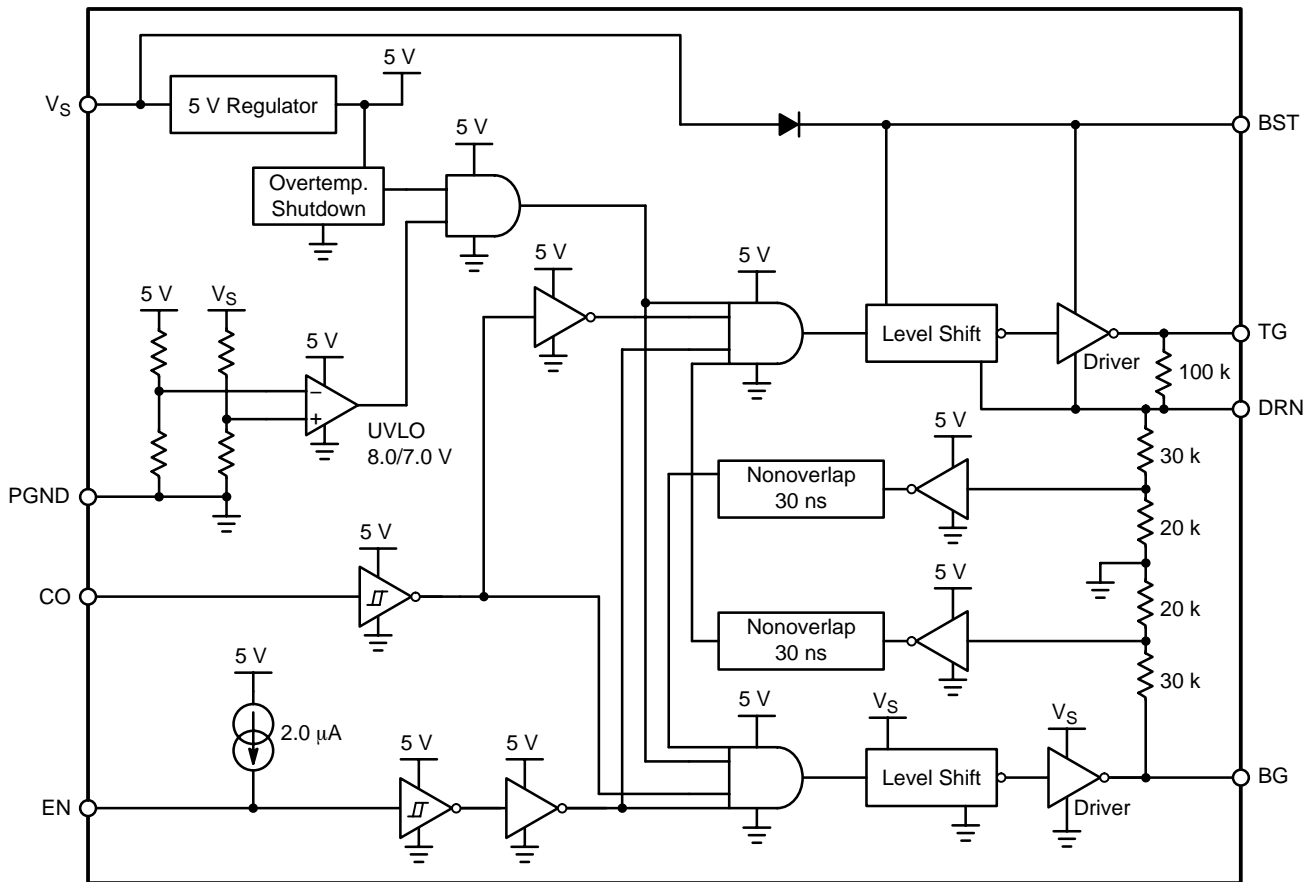


Figure 1. Block Diagram

## PACKAGE PIN DESCRIPTION

Pin	Pin Symbol	Description
1	DRN	The switching node common to the high and low-side FETs. The high-side (TG) driver and supply (BST) are referenced to this pin.
2	TG	Driver output to the high-side MOSFET gate.
3	BST	Bootstrap supply voltage input. In conjunction with an internal diode to VS, a 0.1 μF to 1.0 μF ceramic capacitor connected between BST and DRN develops supply voltage for the high-side driver (TG).
4	CO	Logic level control input produces complementary output states – no inversion at TG; inversion at BG.
5	EN	Logic level enable input forces TG and BG low when EN is low. When EN is high (5.0 V), normal operation ensues. No connect defaults EN high. Note: maximum high input is 5.0 V.
6	VS	Power supply input. A 0.1 μF to 1.0 μF ceramic capacitor should be connected from this pin to PGND.
7	BG	Driver output to the low-side (synchronous rectifier) MOSFET gate.
8	PGND	Ground.

# NCP5355

## MAXIMUM RATINGS

Rating	Value	Unit
Operating Junction Temperature, $T_J$	Internally Limited	$^{\circ}\text{C}$
Package Thermal Resistance: SOIC-8 Junction-to-Case, $R_{\theta JC}$ Junction-to-Ambient, $R_{\theta JA}$	45 165	$^{\circ}\text{C}/\text{W}$ $^{\circ}\text{C}/\text{W}$
Package Thermal Resistance: SOIC-8 EP Junction-to-Ambient, $R_{\theta JA}$ (Note 1)	50	$^{\circ}\text{C}/\text{W}$
Storage Temperature Range, $T_S$	-65 to 150	$^{\circ}\text{C}$
Lead Temperature Soldering: Reflow: (SMD styles only) (Note 2)	230 peak	$^{\circ}\text{C}$
JEDEC Moisture Sensitivity	1	-

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

NOTE: This device is ESD sensitive. Use standard ESD precautions when handling.

1. Ratings applies when soldered to an appropriate thermal area on the PCB.
2. 60 seconds maximum above  $183^{\circ}\text{C}$ .

## MAXIMUM RATINGS

Pin Symbol	Pin Name	$V_{\text{MAX}}$	$V_{\text{MIN}}$	$I_{\text{SOURCE}}$	$I_{\text{SINK}}$
$V_S$	Main Supply Voltage Input	15 V	-0.3 V	NA	2.0 A Peak (< 100 $\mu\text{s}$ ) 250 mA DC
BST	Bootstrap Supply Voltage Input	30 V wrt/PGND 15 V wrt/DRN	-0.3 V wrt/DRN	NA	2.0 A Peak (< 100 $\mu\text{s}$ ) 250 mA DC
DRN	Switching Node (Bootstrap Supply Return)	26 V	-1.0 V DC -5.0 V for 100 ns -6.0 V for 20 ns	2.0 A Peak (< 100 $\mu\text{s}$ ) 250 mA DC	NA
TG	High-Side Driver Output (Top Gate)	30 V wrt/PGND 15 V wrt/DRN	-0.3 V wrt/DRN	2.0 A Peak (< 100 $\mu\text{s}$ ) 250 mA DC	2.0 A Peak (< 100 $\mu\text{s}$ ) 250 mA DC
BG	Low-Side Driver Output (Bottom Gate)	15 V	-0.3 V	2.0 A Peak (< 100 $\mu\text{s}$ ) 250 mA DC	2.0 A Peak (< 100 $\mu\text{s}$ ) 250 mA DC
CO	TG and BG Control Input	5.5 V	-0.3 V	1.0 mA	1.0 mA
EN	Enable Input	5.5 V	-0.3 V	1.0 mA	1.0 mA
PGND	Ground	0 V	0 V	2.0 A Peak (< 100 $\mu\text{s}$ ) 250 mA DC	NA

NOTE: All voltages are with respect to PGND except where noted.

# NCP5355

**ELECTRICAL CHARACTERISTICS** (Note 3) ( $0^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$ ;  $9.2\text{ V} < V_S < 13.2\text{ V}$ ;  $9.2\text{ V} < V_{\text{BST}} < 26\text{ V}$ ;  $V_{\text{EN}} = \text{Float}$ ;  
 $C_{\text{LOAD}} = 3.3\text{ nF}$ ; unless otherwise noted.)

Parameter	Test Conditions	Min	Typ	Max	Unit
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## DC OPERATING SPECIFICATIONS POWER SUPPLY

$V_S$ Quiescent Current, Operating	$V_{\text{CO}} = 0\text{ V}$ or $4.5\text{ V}$ ; No output switching	–	1.0	2.0	mA
$V_{\text{BST}}$ Quiescent Current, Operating	$V_{\text{CO}} = 0\text{ V}$ or $4.5\text{ V}$ ; No output switching	–	3.8	5.0	mA

## UNDERVOLTAGE LOCKOUT

Start Threshold	$V_{\text{CO}} = 0\text{ V}$	7.0	8.0	9.2	V
Stop Threshold	$V_{\text{CO}} = 0\text{ V}$	6.0	7.0	8.0	V
Hysteresis	$V_{\text{CO}} = 0\text{ V}$	0.70	1.00	1.60	V

## CO INPUT CHARACTERISTICS

High Threshold	–	2.0	–	–	V
Low Threshold	–	–	–	0.8	V
Input Bias Current	$0 < V_{\text{CO}} < 5.0\text{ V}$	–	0	1.0	$\mu\text{A}$

## EN INPUT CHARACTERISTICS

High Threshold	Both outputs respond to CO	2.0	–	–	V
Low Threshold	Both outputs are low independent of CO	–	–	0.8	V
Input Bias Current	$0 < V_{\text{EN}} < 5.0\text{ V}$	–7.0	–3.0	+2.0	$\mu\text{A}$

## THERMAL SHUTDOWN

Overtemperature Trip Point	Note 4	150	170	–	$^{\circ}\text{C}$
Hysteresis	Note 4	–	20	–	$^{\circ}\text{C}$

## HIGH-SIDE DRIVER

Peak Output Current	Note 4	–	2.0	–	A
Output Resistance (Sourcing)	Duty Cycle $< 2.0\%$ , Pulse Width $< 100\ \mu\text{s}$ , $T_J = 125^{\circ}\text{C}$ , $V_{\text{BST}} - V_{\text{DRN}} = 12\text{ V}$ , $V_{\text{TG}} = 10\text{ V} + V_{\text{DRN}}$	–	1.0	–	$\Omega$
Output Resistance (Sinking)	Duty Cycle $< 2.0\%$ , Pulse Width $< 100\ \mu\text{s}$ , $T_J = 125^{\circ}\text{C}$ , $V_{\text{BST}} - V_{\text{DRN}} = 12\text{ V}$ , $V_{\text{TG}} = 2.0\text{ V} + V_{\text{DRN}}$	–	1.0	–	$\Omega$

## LOW-SIDE DRIVER

Peak Output Current	Note 4	–	2.0	–	A
Output Resistance (Sourcing)	Duty Cycle $< 2.0\%$ , Pulse Width $< 100\ \mu\text{s}$ , $T_J = 125^{\circ}\text{C}$ , $V_S = 12\text{ V}$ , $V_{\text{BG}} = 10\text{ V}$	–	1.1	–	$\Omega$
Output Resistance (Sinking)	Duty Cycle $< 2.0\%$ , Pulse Width $< 100\ \mu\text{s}$ , $T_J = 125^{\circ}\text{C}$ , $V_S = 12\text{ V}$ , $V_{\text{BG}} = 2.0\text{ V}$	–	1.0	–	$\Omega$

## CHARGE PUMP DIODE

Forward Voltage Drop	$I_D = 100\text{ mA}$	–	1.1	1.4	V
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3. All limits at temperature extremes are guaranteed by characterization using Standard Statistical Quality Control methods.

4. Guaranteed by design, not 100% tested in production.

# NCP5355

**ELECTRICAL CHARACTERISTICS** (Note 5) ( $0^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$ ;  $9.2\text{ V} < V_S < 13.2\text{ V}$ ;  $9.2\text{ V} < V_{\text{BST}} < 26\text{ V}$ ;  $V_{\text{EN}} = \text{Float}$ ;  $C_{\text{LOAD}} = 3.3\text{ nF}$ ; unless otherwise noted.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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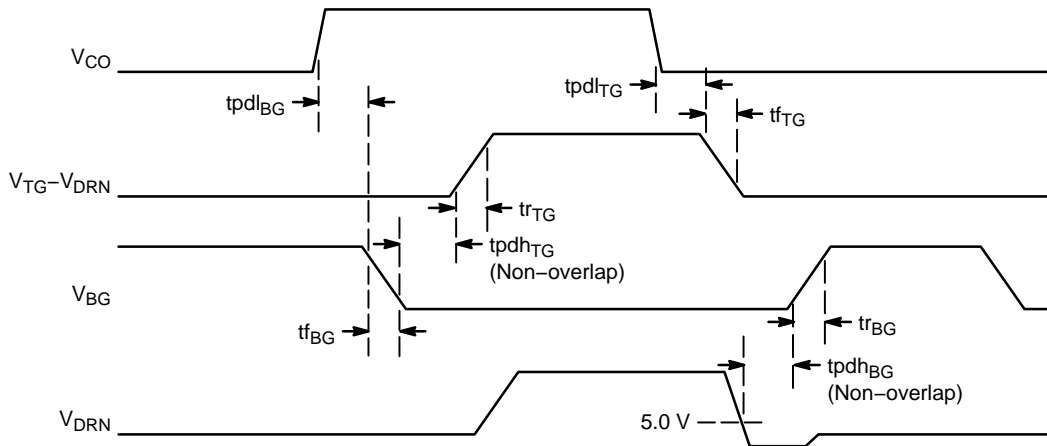
**AC OPERATING SPECIFICATIONS HIGH-SIDE DRIVER**

Rise Time	$t_{r_{\text{TG}}}$	$V_{\text{BST}} - V_{\text{DRN}} = 12\text{ V}$ , $V_S = 12\text{ V}$ (Note 6)	–	15	25	ns
Fall Time	$t_{f_{\text{TG}}}$	$V_{\text{BST}} - V_{\text{DRN}} = 12\text{ V}$ , $V_S = 12\text{ V}$ (Note 6)	–	15	25	ns
Propagation Delay Time, TG Going High (Nonoverlap Time)	$t_{pdh_{\text{TG}}}$	$V_{\text{BST}} - V_{\text{DRN}} = 12\text{ V}$ , $V_S = 12\text{ V}$ (Note 6)	15	30	55	ns
Propagation Delay Time, TG Going Low	$t_{pdl_{\text{TG}}}$	$V_{\text{BST}} - V_{\text{DRN}} = 12\text{ V}$ , $V_S = 12\text{ V}$ (Note 6)	–	45	60	ns

**LOW-SIDE DRIVER**

Rise Time	$t_{r_{\text{BG}}}$	(Note 6)	–	10	20	ns
Fall Time	$t_{f_{\text{BG}}}$	(Note 6)	–	10	20	ns
Propagation Delay Time, BG Going High (Nonoverlap Time)	$t_{pdh_{\text{BG}}}$	(Note 6)	15	30	55	ns
Propagation Delay Time, BG Going Low	$t_{pdl_{\text{BG}}}$	(Note 6)	–	35	55	ns

5. All limits at temperature extremes are guaranteed by characterization using Standard Statistical Quality Control methods.
6. AC specifications are guaranteed by characterization, not 100% tested in production.



**Figure 2. Timing Diagram**



APPLICATIONS INFORMATION

**Enable Pin**

The Enable pin allows logic level On/Off control of the NCP5355. A Logic Level Low (< 0.8 V) disables the part by forcing both TG and BG low. Bringing both gates low prevents the output voltage from ringing below ground at turn-off. A Logic Level High (> 2.0 V) enables the part by allowing CO to control TG and BG.

If the Enable function is not being used, the Enable pin should be left unconnected. This will Enable the part by default, as the Enable pin will be internally pulled high by a 2.0 μA current. The maximum high voltage level is 5.0 V. Voltages greater than this may damage the part.

**Undervoltage Lockout**

Gates TG and BG are both held low until V<sub>s</sub> reaches the UVLO Start Threshold of 8.0 V during startup. V<sub>s</sub> exceeding the UVLO threshold allows CO to take control of both gates. If V<sub>s</sub> falls below the UVLO Stop Threshold of 7.0 V, both gates are then forced low until V<sub>s</sub> again exceeds the Start Threshold.

**Supply Capacitor Selection**

A 1.0 μF ceramic capacitor (C<sub>VS</sub> in Figure 4) should be located close to the V<sub>s</sub> supply pins to provide peak current and to reduce noise. A small 1.0 Ω to 5.0 Ω resistor (R<sub>VS</sub> in Figure 4) may also be added in series with C<sub>VS</sub> to provide additional filtering in noisy environments.

**Bootstrap Capacitor Selection**

The size of the Top MOSFET bootstrap capacitor (C<sub>BST</sub> in Figure 4) is determined from the following equation:

$$C_{BST} \geq \frac{Q_{TtopFETs}}{\Delta V_{BST}}$$

where

Q<sub>TtopFETs</sub> is the sum of the Top MOSFETs total gate charge,

ΔV<sub>BST</sub> is the maximum change in voltage across the bootstrap capacitor and is typically designed for a drop of less than a 1.0 V.

For example, a circuit using one Top MOSFET with a typical Q<sub>TtopFETs</sub> of 60 nC (at 12 V V<sub>gs</sub>) and 1.0 V of droop would give a minimum value for C<sub>BST</sub> of 60 nF.

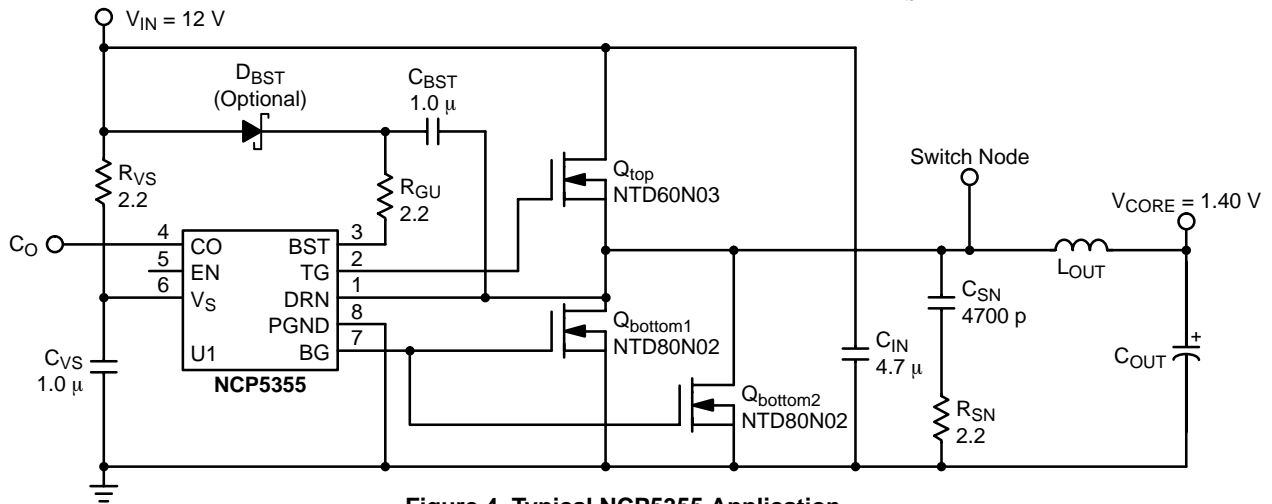


Figure 4. Typical NCP5355 Application

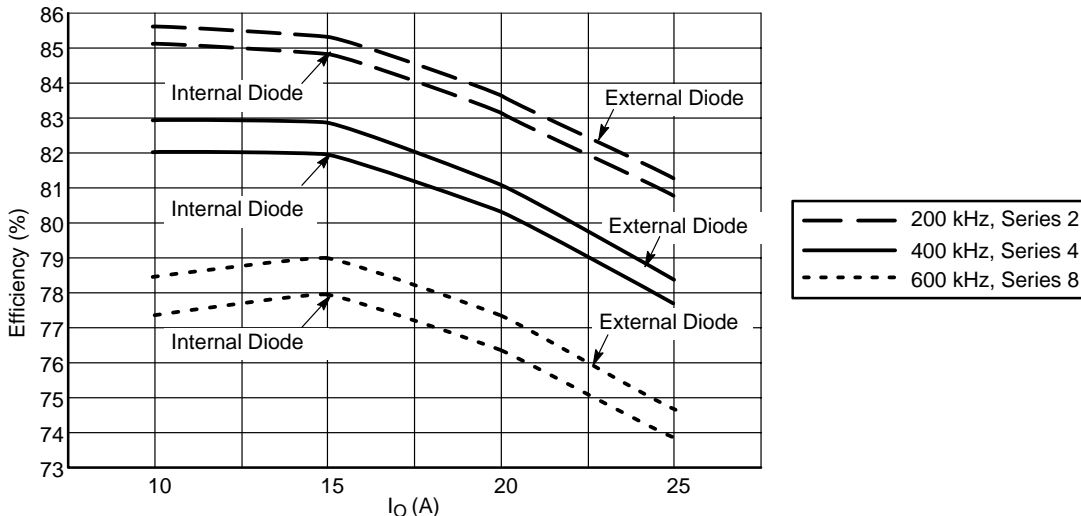


Figure 5. Efficiency With and Without an Added External Bootstrap Diode, See Figure 4 for Test Circuit

**Internal or External Bootstrap Diode**

For convenience, a bootstrap diode is internally provided by the NCP5355. This internal diode reduces system cost and parts count.

However, this diode will have higher losses than a standard small signal switching or Schottky diode. By using an external Schottky diode (DBST in Figure 4) a small improvement in efficiency can be achieved as illustrated by the graph in Figure 5.

While the difference in efficiency is relatively small, this difference represents heat loss in the driver and on average driver temperature may be reduced by about 10°C if using an external diode. If an external diode is used, it should be a Schottky or switching diode. (For example: ON Semiconductor Part Number BAT54HT1 or BAS16HT1.)

**Adaptive Nonoverlap**

The NCP5355 includes adaptive nonoverlap protection to prevent top and bottom MOSFET cross conduction.

When CO goes low signaling TG to turn off the top MOSFET, BG does not go high until the switch node (DRN pin) has fallen below 5.0 V and a fixed amount of delay (tpdhBG) has elapsed. This ensures that the top MOSFET is off before the bottom MOSFET is turned on.

When CO goes high signaling BG turn off the Bottom MOSFET, TG does not go high until BG has fallen below a threshold of 5.0 V and a fixed amount of time has elapsed (tpdhTG).

However, caution must be observed if too much gate resistance and inductance is introduced into the path between the IC and the gate of the low MOSFET. A condition can occur where the NCP5355 will sense that BG has fallen below 5.0 V while the gate end of the MOSFET still has not fallen low enough to turn off the device. This parasitic gate impedance between the driver and MOSFET can reduce the nonoverlap time, and result in shoot-through currents.

**Power Dissipation**

Driver power dissipation may be approximated by the following equation:

$$P_{loss} = f_{SW} \cdot V_s \cdot (1.5 \cdot Q_{TtopFETs} + Q_{TbottomFETs}) + V_s \cdot I_s$$

where

- f<sub>SW</sub> is the switching frequency,
- V<sub>s</sub> is the supply voltage,
- Q<sub>TtopFETs</sub> is the sum of the Top MOSFETs total gate charge,
- Q<sub>TbottomFETs</sub> is the sum of the Bottom MOSFETs total gate charge
- I<sub>s</sub> is the supply quiescent current, typically around 5.0 mA

The 1.5 factor is a result of the internal bootstrap diode whose loss is equivalent to the charge lost in turning on the Top MOSFET. If an external diode is used to improve efficiency, the 1.5 factor is replaced with 1.0 as this loss will now occur outside the package.

Safe design practice requires limiting the SO8 device power dissipation to around 700 mW. Higher frequency designs may require limiting the supply voltage (V<sub>s</sub>) to less than 12 V to maintain this limit.

**Switch Node Overshoot and Ringing**

Due to the high current sourcing capability of the NCP5355, increased overshoot and ringing may be noticed at the switch node (DRN pin). This can be reduced in several ways.

One is by adding a low ESR 1.0 μF–10 μF ceramic capacitor (C<sub>IN</sub> in Figure 4) from V<sub>IN</sub> to ground near each Q<sub>top</sub>. This capacitor should be located in such a manner as to reduce the loop area of the switch node as shown in Figure 6. A smaller loop area from C<sub>IN+</sub> to Q<sub>top</sub> to Q<sub>bottom</sub> and back to C<sub>IN-</sub> will reduce the amount of ringing by reducing the PCB inductance. If further reduction in overshoot and ringing is desired, a Top MOSFET gate drive resistor may be added (R<sub>GU</sub> in Figure 4) to slow the turn-on of the Top MOSFET without increasing the turn-off time.

**Layout Guidelines**

When designing any switching regulator, the layout is very important for proper operation. Gate drivers experience high di/dt during switching, and the inductance of the gate drive traces need to be minimized. Gate drive traces should be kept as short and wide (25 to 30 mils) as practical, and should have a return path directly below the gate trace. The use of a ground plane is a desirable way to return ground signals. Component location is very important. The boost and the V<sub>s</sub> capacitor are the most critical, and need to be placed as close as possible to the driver IC pins (C<sub>Vs</sub> and C<sub>BST</sub> in Figure 4) as shown in Figure 6. Higher frequency designs will magnify any layout problems, and added attention to these guidelines should be observed in designs above 250 kHz.

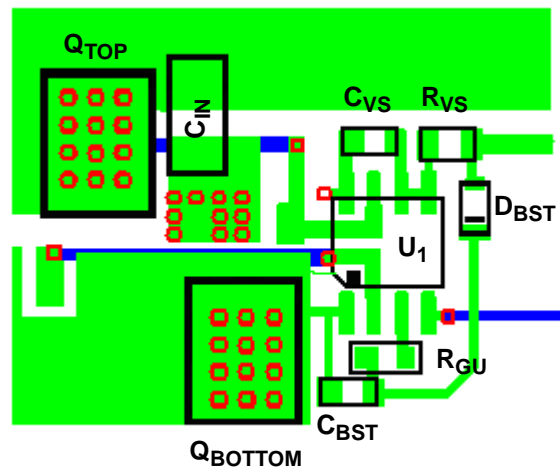


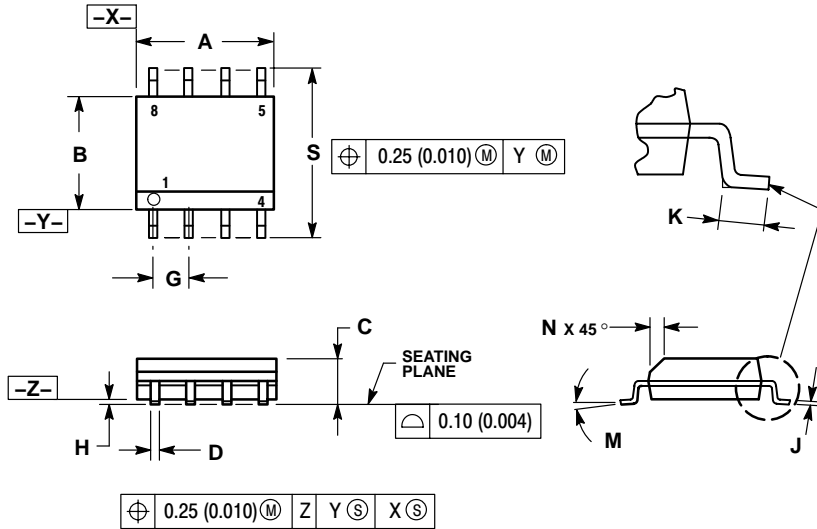
Figure 6. Typical NCP5355 PCB Layout



# NCP5355

## PACKAGE DIMENSIONS

SOIC-8  
D SUFFIX  
CASE 751-07  
ISSUE AD

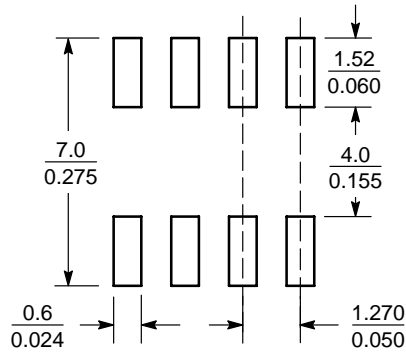


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### SOLDERING FOOTPRINT\*



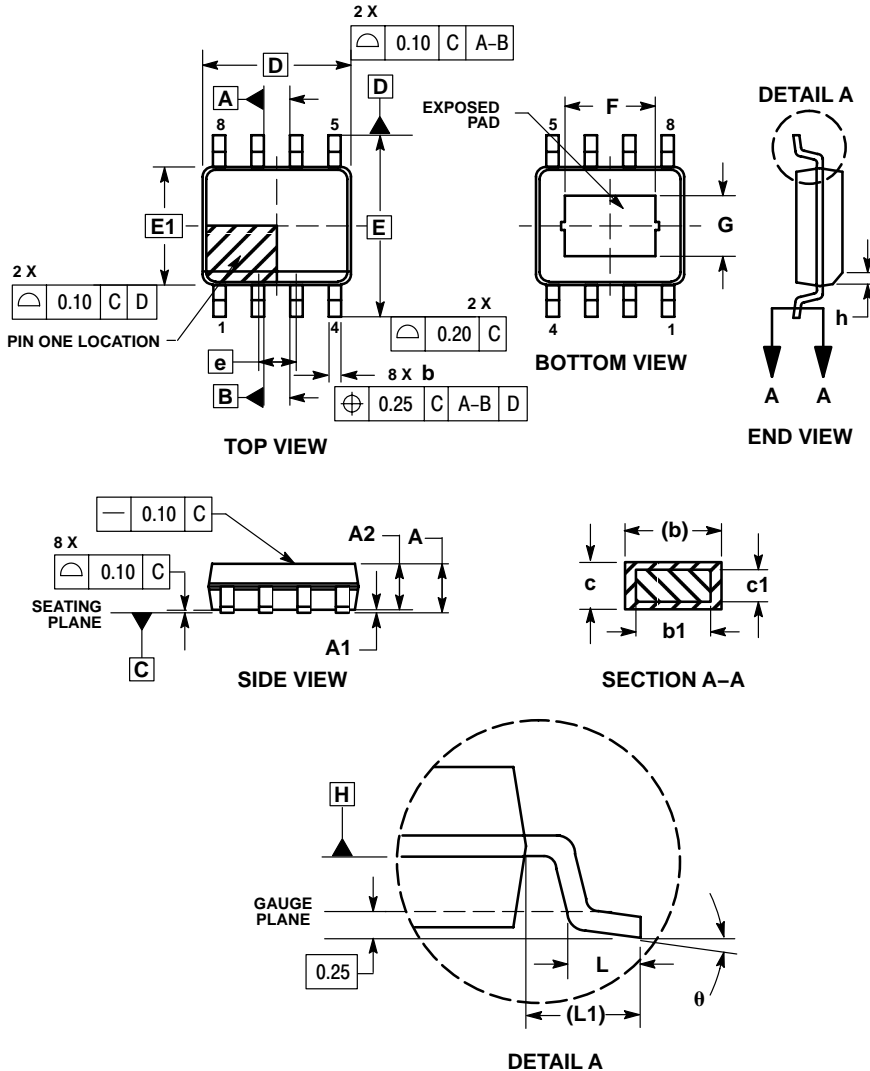
SCALE 6:1 (mm/inches)

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NCP5355

## PACKAGE DIMENSIONS

SOIC-8 EP  
CASE 751AC-01  
ISSUE O



### NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS (ANGLES IN DEGREES).
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.00	0.10
A2	1.35	1.65
b	0.31	0.51
b1	0.28	0.48
c	0.17	0.25
c1	0.17	0.23
D	4.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
L1	1.04 REF	
F	2.24	3.20
G	1.55	2.51
h	0.25	0.50
θ	0°	8°

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